EE204 Design Homework

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1 Overview of the assignment

- The aim of this assignment is to design an **NGSPICE code** to simulate the functionality of a **single-ended differential amplifier** which is further used as an op-amp.
- Furthermore, this assignment involves the application of the code in order to simulate other circuit such as the inverting amplifier, filters of various sorts, the Wien bridge and cross-coupled oscillators, and negative differential resistance.

2 Components

The nMOS and pMOS Field Effect Transistors (FETs) are used throughout the differential amplifier. For later parts such as the inverting amplifier, filters etc, resistors and capacitors are suitably used.

3 Design

The differential amplifier utilises a voltage-biased MOSFET as the common current source at the common source. Furthermore, it uses a cascode arrangement of MOSFETs. In order to increase the gain, the drain side consists of a cascode current mirror as well.

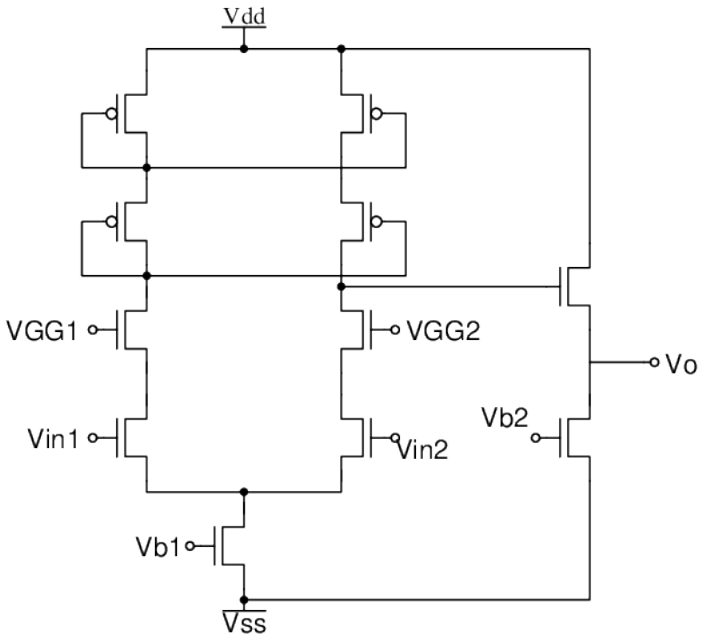


Figure 1: Differential Amplifier - Circuit Diagram

In the above described differential amplifier, the following values were used:

$$V_{DD} = 5V;\ V_{SS} = -5V$$

$$V_{b_1} = V_{b_2} = V_{SS} + 1 = -4V;$$

$$V_{GG_1} = V_{GG_2} = V_{DD} - 2 = 3V$$

The differential amplifier is considered as an operational amplifier (op-amp) for the remaining part of the assignment. The inverting amplifier provides a gain of -2 having $R_1 = 100\Omega$ and $R_2 = 200\Omega$.

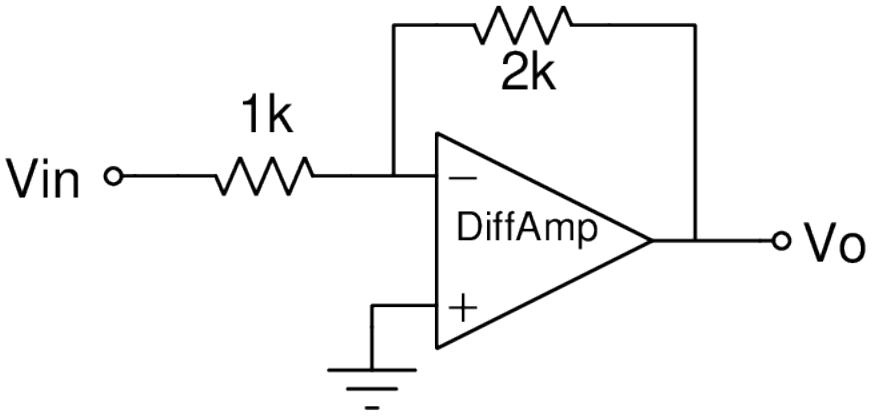
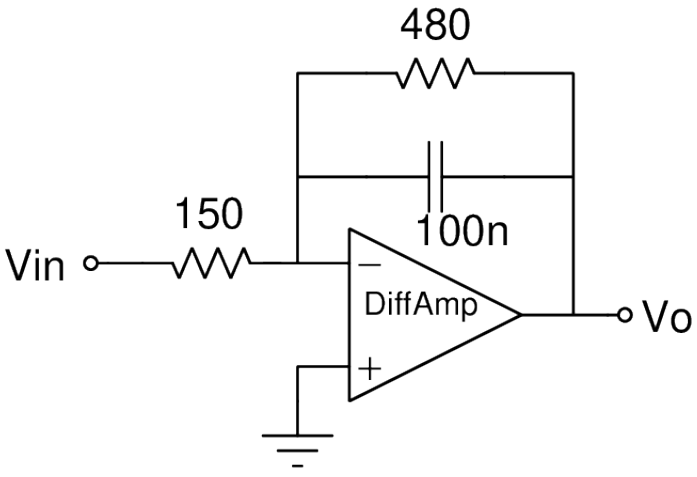
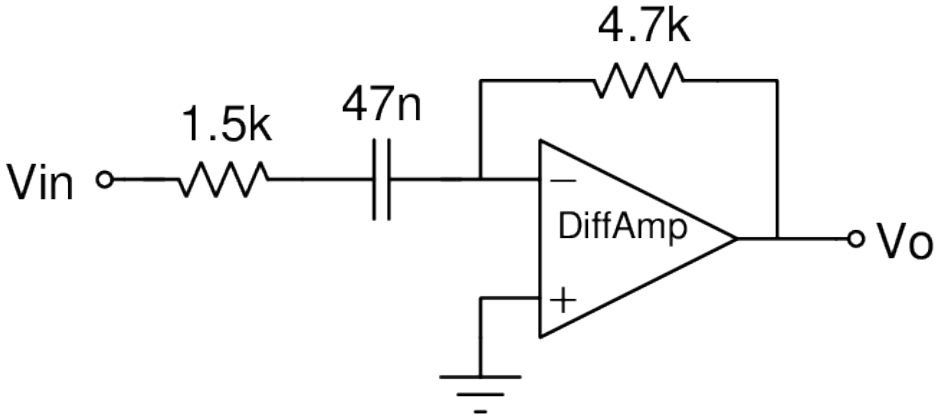


Figure 2: Inverting Amplifier - Circuit Diagram

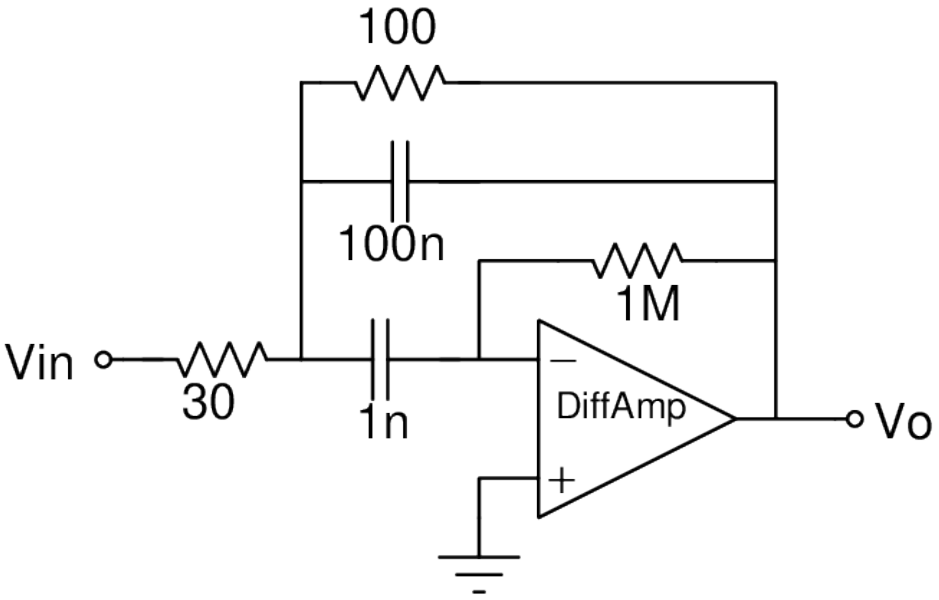
Following the inverting amplifier, three filters are designed - a low-pass filter of cutoff frequency 1kHz, a high-pass filter of cutoff frequency 10kHz and a band-pass filter of passband 1kHz to 10kHz.



(a) Low Pass Filter - Circuit Diagram



(b) High Pass Filter - Circuit Diagram



(c) Band Pass Filter - Circuit Diagram

Figure 3: Filters

A Wien bridge oscillator with a frequency of 1kHz is designed as follows:

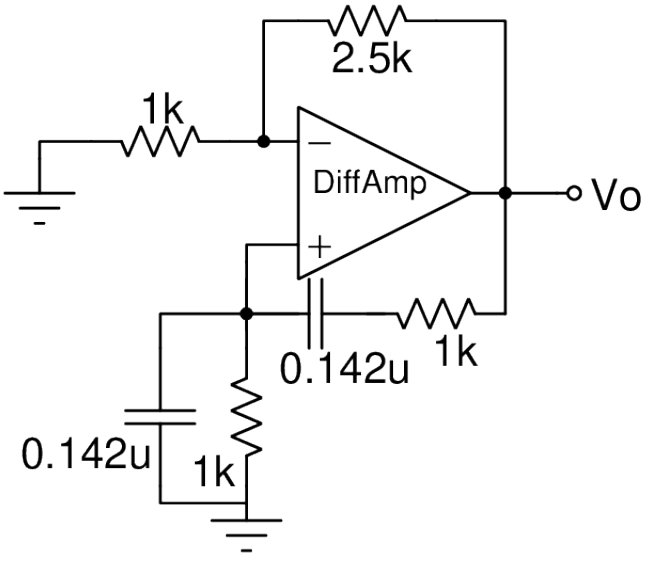


Figure 4: Wien Bridge Oscillator - Circuit Diagram

Furthermore a cross-coupled oscillator with a frequency of 1kHz is designed as shown below:

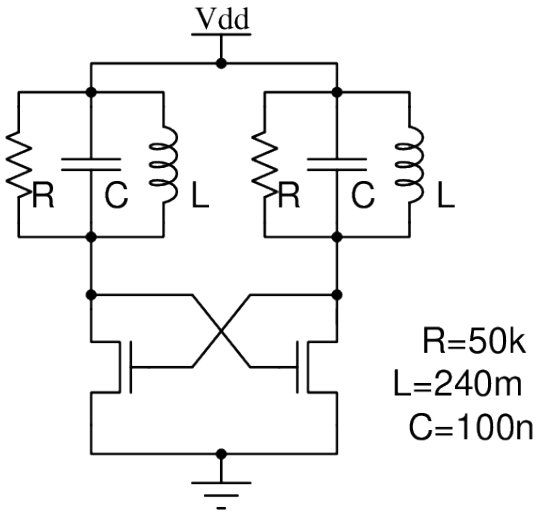


Figure 5: Cross Coupled Oscillator - Circuit Diagram

Finally, a negative differential resistance is simulated very similar to the model provided in the end-semester examination:

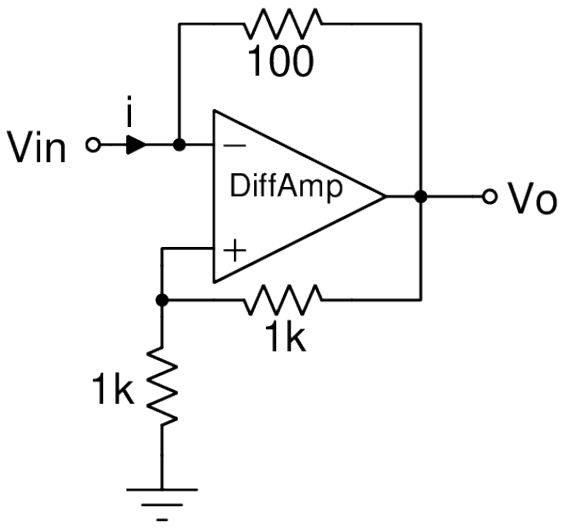


Figure 6: Negative Differential Resistance - Circuit Diagram

The resistance which is supposed to be negated is kept as 100Ω

4 Codes and Plots

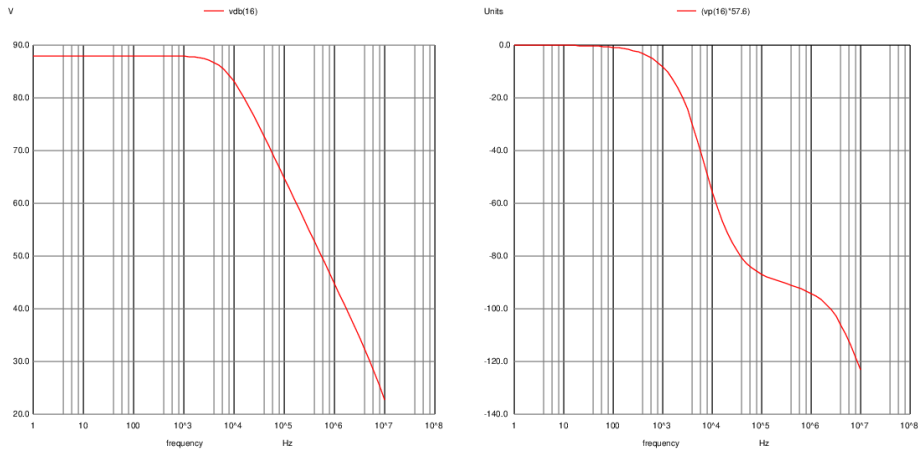
The TSMC Models for the nMOS and pMOS transistors provided in the beginning of the semester was used, utilising the models hence provided.

4.1 Differential Amplifier

```
*Differential Amplifier and Voltage Follower

.include TSMC_Model.txt
VDD   1  0  5
VSS  13  0 -5
Vb1  12 13  1
Vb2  17 13  1
Vin1  9  0 ac 1 dc 0
```

```
Vin2 10  0  0
VGG1  1  8  2
VGG2  1  7  2
Ma  11 12  13 13 CMOSN
Mb1  5  9  11 13 CMOSN
Mb2  6 10  11 13 CMOSN
Mc1  2  7   5 13 CMOSN
Mc2  4  8   6 13 CMOSN
Md1  2  2  14  1 CMOSP
Md2  4  2  15  1 CMOSP
Me1 14 14   1  1 CMOSP
Me2 15 14   1  1 CMOSP
Ms1  1  4  16 13 CMOSN W=30u L=1u
Ms2  16 17 13 13 CMOSN W=30u L=1u

.ac dec 10 1 10000k
.control
run
plot vdb(16) xlog
plot (vp(16)*57.6) xlog    * converts radians to degrees as well
.endc
.end
```

The Bode plots hence obtained from the differential amplifier on varying the frequency of the input proves that the gain in the pass band is more than 10^4. In order to reduce the output impedance, a source follower is used. The code for the measurement of the output impedance follows in Section 4.3.



(a) Gain (b) Phase

Figure 7: Bode Plots for the Differential Amplifier

4.2 Subcircuit from Differential Amplifier

```
*Differential Amplifier and Voltage Follower

.subckt DIFFAMP 9 10 1 13 16
.include TSMC_Model.txt
Vb1   12 13   1
Vb2   17 13   1
VGG1   1   8   2
VGG2   1   7   2
Ma   11 12   13 13 CMOSN
Mb1   5   9   11 13 CMOSN
Mb2   6 10   11 13 CMOSN
Mc1   2   7    5 13 CMOSN
Mc2   4   8    6 13 CMOSN
Md1   2   2   14   1 CMOSP
Md2   4   2   15   1 CMOSP
Me1 14 14    1   1 CMOSP
Me2 15 14    1   1 CMOSP
Ms1   1   4   16 13 CMOSN w = 30u l = 1u
Ms2   16 17 13 13 CMOSN w = 30u l = 1u
```

```
.ends DIFFAMP
```

4.3 Output Resistance Calculation

```
*Output Resistance Calculation

.include DiffAmp.txt
VDD   1  0  5
VSS   2  0 -5
Vp    3 0 0
Vm    4 0 0
Vo    5 0 sin(0 10m 100 0 0)
x1   3 4 1 2 5 DIFFAMP
.tran 0.02m 50m
.control
run
plot v(5) vs i(Vo)
.endc
.end
```

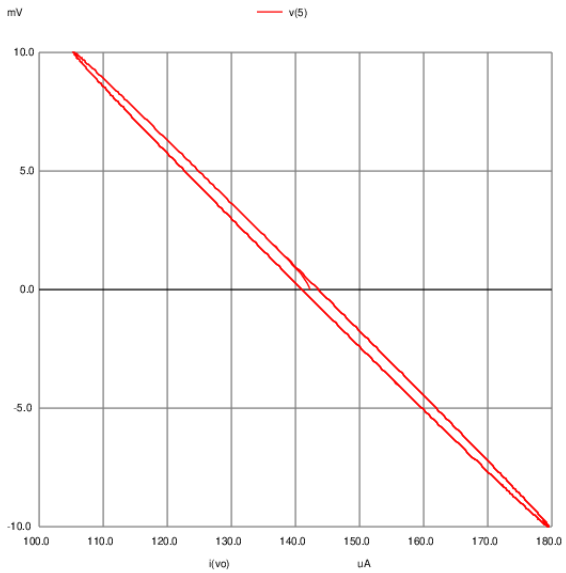


Figure 8: Output Resistance Calculation

As is observed form the above given plot, the output impedance of the complete circuit is approximately $-\frac{10mV-(-10mV)}{105\mu A-180\mu A}$ which lies in the range of 100Ω, hence being satisfactorily good for the differential amplifier.

4.4 Inverting Amplifier

```
*Inverting Amplifier

.include DiffAmp.txt
VDD   1  0  5
VSS   2  0 -5
Vp    3 0 0
Vm    6 0 ac 1 dc 0
x1   3 4 1 2 5 DIFFAMP
R1    4 5 2k
R2    4 6 1k

.ac dec 10 1 100k
.control
run
plot vdb(5) xlog

.endc
.end
```

As can be observed from the below provided plot, the output has a gain of 6dB (approximately 2 in the linear scale) and the output is inversed. Hence, the gain of the inverting amplifier is -2 as expected.
(The plot shows an increase in the gain after 10kHz. However this increase is very small and the gain tends to sink beyond a larger frequency as expected)

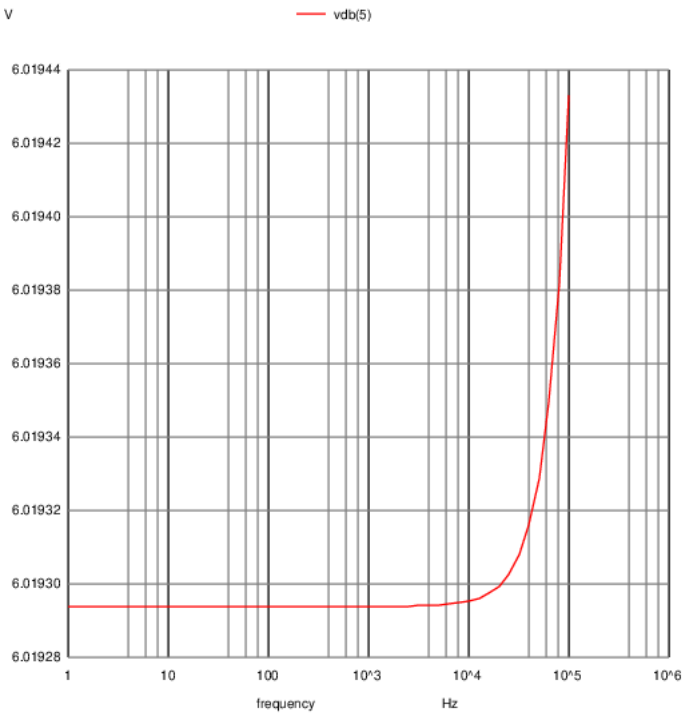


Figure 9: Inverting Amplifier

4.5 Filters

4.5.1 Low Pass Filter

```
*Low Pass Filter

.include DiffAmp.txt
VDD    1   0   5
VSS    2   0 -5
x1     3 4 1 2 5 DIFFAMP
Vp     3 0 0
Vm     6 0 ac 1 dc 0
R1     4 6 150
R2     4 5 480
C1     4 5 100n
.ac dec 10 1 500k
```

```
.control
run
plot vdb(5) xlog

.endc
.end
```

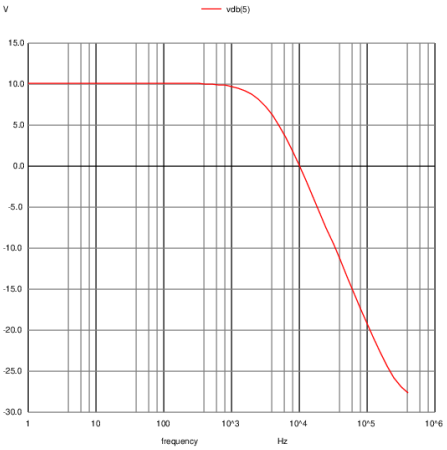
4.5.2 High Pass Filter

```
*High Pass Filter

.include DiffAmp.txt
VDD   1  0  5
VSS   2  0 -5
x1    3 4 1 2 5 DIFFAMP
Vp    3 0 0
Vm    6 0 ac 1 dc 0
R1    7 6 1.5k
R2    4 5 4.7k
C1    4 7 47n
.ac dec 10 1 5000k
.control
run
plot vdb(5) xlog

.endc
.end
```

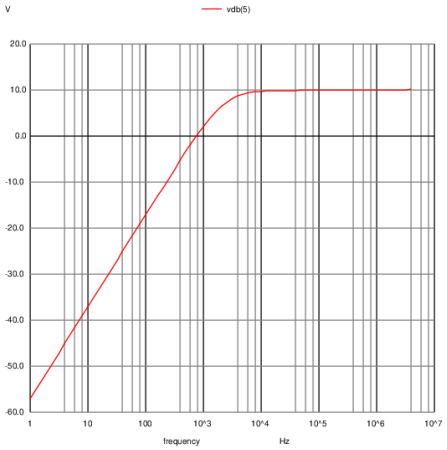
4.5.3 Band Pass Filter

```
*Band Pass Filter

.include DiffAmp.txt
VDD   1  0  5
VSS   2  0 -5
x1    3 4 1 2 5 DIFFAMP
Vp    3 0 0
Vm    6 0 ac 1 dc 0
```

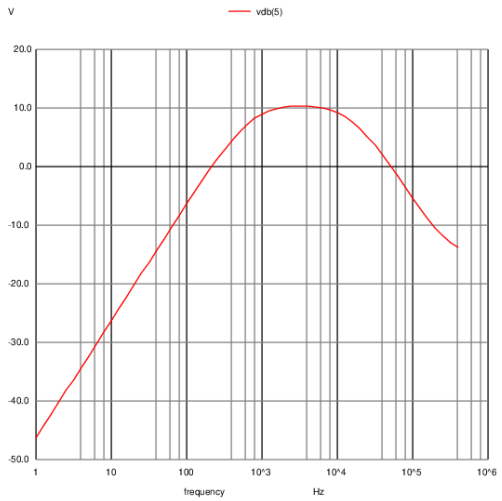
```
R1     7 6 30
R2     5 4 1Meg
C1     4 7 1n
C2     5 7 100n
R3     5 7 100
.ac dec 10 1 500k
.control
run
plot vdb(5) xlog

.endc
.end
```



(a) Low Pass Filter Characteristics



(b) High Pass Filter Characteristics



(c) Band Pass Filter Characteristics

Figure 10: Filters

4.6 Oscillators

4.6.1 Wien Bridge Oscillator

```
*Wien Bridge Oscillator

.include DiffAmp.txt
VDD   1  0  5
VSS   2  0 -5
x1    3 4 1 2 5 DIFFAMP
Ra    3 0 1k
Rb    6 5 1k
Ca    3 0 0.142u
Cb    3 6 0.142u
R1    4 5 2.5k
R2    4 0 1k
.tran 100u 110m 100m
.control
run
plot v(5)
```

```
.endc
.end
```

A fragment of the wave obtained at the output is shown below:

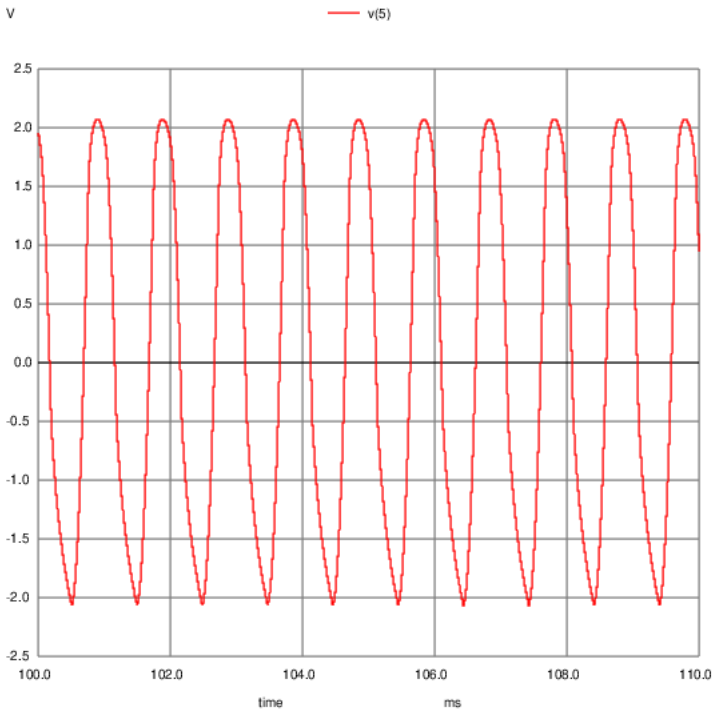


Figure 11: Wien Bridge Oscillator Fragment

4.6.2 Cross-Coupled Oscillator

```
*Cross-Coupled Oscillator

.include TSMC_Model.txt
VDD    1   0   5
VSS    2   0  -5
Ra     1   3   50k
Ca     1   3   100n
La     1   3   240m
```

```
Rb     1   4   50k
Cb     1   4   100n
Lb     1   4   240m
M1     3   4   0 2 CMOSN
M2     4   3   0 2 CMOSN
.tran 5u 610m 600m
.control
run
plot v(4)

.endc
.end
```

A fragment of the wave obtained at the output is shown below:

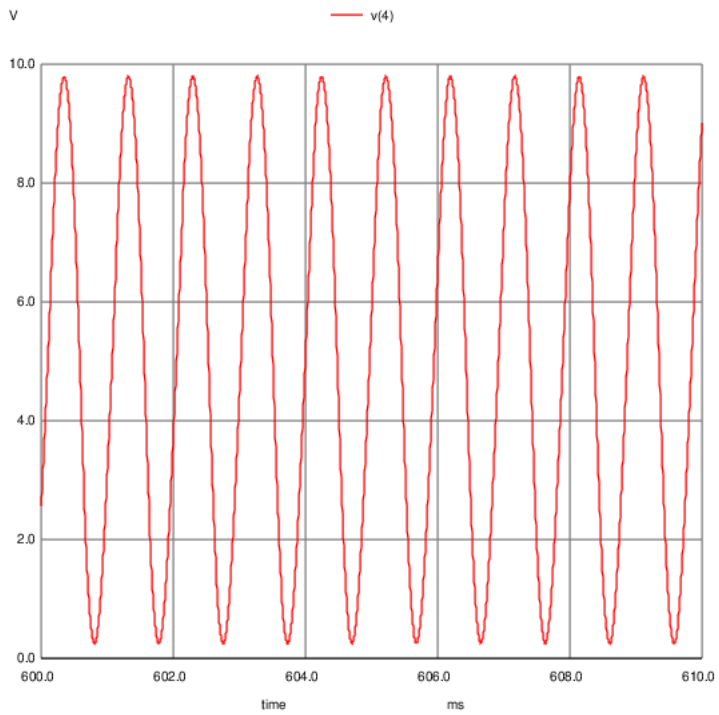


Figure 12: Cross-Coupled Oscillator Fragment

The mean voltage is at 5V (V_{DD}) possibly because, $V_{DD} = 5V$ and $V_{SS} = 0V = GND$, which causes a bias in the output.

4.7 Negative Differential Resistance

```
*Negative Differential Resistance

.include DiffAmp.txt
VDD    1   0   5
VSS    2   0 -5
x1     3 4 1 2 5 DIFFAMP
Vin    3 0 sin(0 100m 1k 0 0)
R      3 5 100
R1     4 5 1k
R2     4 0 1k
.tran 5u 1
.control
run
plot v(3) vs v(3)/100-v(5)/100

.endc
.end
```

In the above given code, the V-I characteristics is plotted by plotting $V\ vs\ \frac{\Delta V}{R}$. Hence the following plot is obtained.

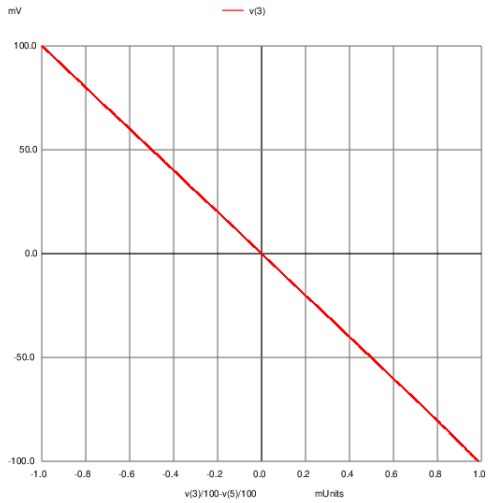


Figure 13: Negative Differential Amplifier - V-I Characteristics

As is visible in the plot, the slope of the V-I curve is obtained as approximately -100Ω, which is also -R.

5 Conclusion

From the above simulation of a differential amplifier and several circuits based on the same amplifier, we may conclude that the formerly described differential amplifier behaves a lot like an operational amplifier (op-amp). This is clearly visible since all the circuits hence defined show almost perfect match with the equivalents made from an operational amplifier.
Moreover, on performing the above assignment, several knowledgeable points were tested such as conditions for oscillation, formulae for cutoff frequency and how to increase the gain and bandwidth of the differential amplifier.